IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:

Leo Mathew et al.

Group Art Unit:

Application No.: Date Filed:

Unassigned

Examiner:

Unassigned

Title:

INTEGRATED CIRCUIT HAVING MULTIPLE MEMORY TYPES AND

METHOD OF FORMATION

INFORMATION DISCLOSURE STATEMENT (IDS)

Commissioner For Patents Alexandria, VA 22313

b. 🔲

SIR:

In accordance with 37 C.F.R. §1.56 and in compliance with 37 C.F.R. §§1.97 and 1.98, the references listed on attached Form PTO/SB/08 and/or subsequently identified herein, are for consideration by the United States Patent and Trademark Office. Pursuant to the Office waiving the requirement under 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC §371 after June 30, 2003, copies of the reference are not submitted herewith.

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I.	COPIE a. 🛛	A legible copy of (i) each foreign patent; (ii) each to be listed; and (iii) all other information or included herewith.	
	b. 🗌	Any patents, publications or other information wenclosed herewith were previously cited by or sapplications which has been relied upon for an ea	ubmitted to the PTO in one of the following
		U.S. Serial Number	U.S. Filing Date
II.	CONC a. ⊠	ISE EXPLANATION OF THE RELEVANCE (che Except as may be indicated below in (b) of this so information are in the English language (concise	ection, all of the patents, publications or other

c. The following additional information is provided for the Examiner's consideration:

CROSS REFERENCE TO RELATED APPLICATION(S)

The Examiner is advised that the following co-pending application(s) contain(s) subject matter that may be related to the present application. By bringing this (these) applications to the Examiner's attention,

A concise explanation of the relevance of all patents, publications or other information listed

Serial No.	Filing Date	Art Unit
10/074,732	09-03-2002	2815
10/427,141	04-30-2003	2811
10/443,375	05-22-2003	1765
10/443,908	05-22-2003	2818

Applicant(s) does(do) not waive the confidentiality provisions of 35 U.S.C. §122.

that is not in the English language is as follows:

FEES

IV. 🔀	a.□	within three months of the filing date of a national application other than a continued prosecution application under § 1.53(d) (37 C.F.R. §1.97(b)(1)). No fee or statement is
	b.	required. within three months of the date of entry of the national stage as set forth in § 1.491 in an international application (37 C.F.R. §1.97(b)(2)). No fee or statement is required.
	c.🛛	before the mailing date of a first Office Action on the merits (37 C.F.R. §1.97(b)(3)). No fee or statement is required.
	d.	before the mailing date of a first Office Action after the filing of a request for continued examination under § 1.114 (37 C.F.R. § 1.97(b)(4)). No fee or statement is required.
V. 🗌	before t	OS IS BEING FILED UNDER 37 C.F.R. §1.97(c): (check one box) the mailing date of any of a Final Office Action under 37 C.F.R. §1.113, a Notice of Allowance 7 C.F.R. §1.311, or an action that otherwise closes prosecution in the application (See 37 C.F.R.
	a. b.	No statement; therefore, charge deposit account 502117 the fee set forth in 37 C.F.R. §1.17(p). See the statement below. No fee is required.
VI. 🔲	THIS II	OS IS BEING FILED UNDER 37 C.F.R. §1.97(d):
		fore payment of the issue fee and is accompanied by the following:
	1)	a statement under 37 C.F.R. §1.97(e) as provided below; and
	2)	charge deposit account 502117 the petition fee set forth in §1.17(p).
VII. 🔲		MENT UNDER 37 C.F.R. §1.97(e) (check only one box, if applicable) dereigned hereby states that
	a. 🗌	each item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of IDS; or
	b. <u> </u>	no item of information contained in the IDS was cited in a communication from a foreign Patent Office in a counterpart foreign application, and to knowledge of the person signing the statement after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 C.F.R. 1.56(c) more than three months prior to the filing of this statement, or
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VIII.	PAYMI	Please of fee(s). If Appli Commis	c in the amount of	is enclosed for the above-identified fee(s). 117 in the amount of \$180.00 for the above-indicated litional fees, or if any overpayment has been made, the to credit or debit Deposit Account 502117. ed for Deposit Account charges and debits.
	te statuto	ry prior		the interests of candor and without any admission that they anticipates the invention or which would render the same of ordinary skill in the art.
	determine he prope	d that th	is IDS has been filed under	g this IDS, he/she is requested to contact the undersigned. the wrong rule, the PTO is requested to consider this IDS and charge the appropriate fee to Deposit Account No.
				Respectfully submitted, Leo Mathew et al. Robert L. King
	ROLA, II er Numb			Robert L. King Attorney for Applicant(s) Reg. No. 30,185 Tel. 512-996-6839
Enclosu	ires:		PTO/SB/08 References A-19 thru A-34 Foreign Search Report Other:	

PTO/SB/08A (04-03)

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			Application Number		
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STATEMI	NT BY APPLICA	NT	First Named Inventor	Leo Mathew et al.	
017.12		•••	Group Art Unit	Unassigned	
(use as many sheets as nec	essary)		Examiner Name	Unassigned	
Sheet 1	of	3	Attorney Docket Number	SC13161TP	

			J. S. PATENT DOCU	MENTS	-
Examiner Initials*	Cite No. 1	Document Number Number -Kind Code² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A-1	US - 6,583,469	06-24-2003	Fried et al.	
	A-2	US - 2003/113970 A1	06-19-2003	Fried et al.	
	A-3	US - 6,472,258	10-29-2002	Adkisson et al.	
	A-4	US - 6,458,662	10-01-2002	'Yu	
	A-5	US - 6,433,609	08-13-2002	Voldman	
	A-6	US - 6,414,356	07-02-2002	Forbes et al.	
	A-7	US - 6,413,802	07-02-2002	Hu et al.	
	A-8	US - 6,396,108	05-28-2002	Krivokapic et al.	
	A-9	US - 6,372,559	04-16-2002	Crowder et al.	
•	A-10	US - 6,355,961	03-12-2002	Forbes	
	A-11	US - 6,330,184	12-11-2001	White et al.	
	A-12	US - 6,300,182	10-09-2001	Yu	
	A-13	US - 6,097,065	08-01-2000	Forbes et al.	
	A-14	US - 6,150,687	11-21-2000	Noble et al.	
	A-15	US - 6,011,725	01-04-2000	Eitan	
	A-16	US - 5,804,848	09-08-1998	Mukai	
	A-17	US - 5,689,127	11-18-1997	Chu et al.	
	A-18	US -4,859,623	08-22-1989	Busta	
		US-			
		US -			

Examiner	Date	
Signature	Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form

¹ Unique citation designation number. ² See Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.

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Substitute for to	nm 1449A/PTO			C	omplete if Known	
				Application Number		
11	NFORMATION DISC	CLOSU	RE	Filing Date		
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Sheet	2	of	3	Attorney Docket Number	SC13161TP	

-19	Related Application 10/074,732 entitle	TTERS), title of the a , page(s), volume-issu	ticle (when appropriate), title of the ue number(s), publisher, city and/o	or country where published.	T 6		
Cite No. 1	NON PATENT LITE Include name of the author (in CAPITAL LE symposium, catalog, etc.), date, Related Application 10/074,732 entitle	ERATURE DOCUM TTERS), title of the a. page(s), volume-issu	Marso et al. ENTS ticle (when appropriate), title of the enumber(s), publisher, city and/o	or country where published.	ial,		
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A-21		1411-11-1-1-1					
	Related Application 10/074,732 entitled "Method of Forming a Vertical Double Gate Semiconductor Device and Structure Thereof" filed September 3, 2002 entitled						
A-22	Related Application 10/443,375 entitled "Transistor With Independent Gate Structures" filed May 22, 2003						
A-23	Related Application 10/443,908 "Memory with Charge Storage Locations" entitled filed May 22, 2003						
A-24	Related Application 10/427,141 entitled "Semiconductor Fabrication Process with Asymmetrical Conductive Spacers" filed April 30, 2003						
A-25	LEE et al.; "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI"; IEEE Electron Device Letters, 2002; pp 1-3 and 208-209.						
A-26	YU, BIN et al; "FinFET Scaling to 10nr	m Gate Length:; I	EEE IDEM 2002; pp 251-25	54; IEEE			
A	-23 -24 -25	-23 Related Application 10/443,908 "Mem- -24 Related Application 10/427,141 entitle Spacers" filed April 30, 2003 -25 LEE et al.; "Multilevel Vertical-Channe pp 1-3 and 208-209.	Related Application 10/443,908 "Memory with Charge S Related Application 10/427,141 entitled "Semiconducto Spacers" filed April 30, 2003 LEE et al.; "Multilevel Vertical-Channel SONOS Nonvol pp 1-3 and 208-209.	Related Application 10/443,908 "Memory with Charge Storage Locations" entitled Related Application 10/427,141 entitled "Semiconductor Fabrication Process with Spacers" filed April 30, 2003 LEE et al.; "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI"; IEE pp 1-3 and 208-209.	Related Application 10/443,908 "Memory with Charge Storage Locations" entitled filed May 22, 2003 Related Application 10/427,141 entitled "Semiconductor Fabrication Process with Asymmetrical Conductive Spacers" filed April 30, 2003 LEE et al.; "Multilevel Vertical-Channel SONOS Nonvolatile Memory on SOI"; IEEE Electron Device Letters, 20 pp 1-3 and 208-209.		

Examiner	Date	
Signature	Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation, if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Unique citation designation number. ² See Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English Language Translation is attached.

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Substitute for	r form 1449A/PTO				omplete if Known	
				Application Number		
	INFORMATION	I DISCLOSU	JRE	Filing Date		
	STATEMENT I	RY APPLICA	NT	First Named Inventor	Leo Mathew et al.	
	(use as many sheets as necessary)			Group Art Unit	Unassigned	
(use as many				Examiner Name	Unassigned	
Sheet	3	of	3	Attorney Docket Number	SC13161TP	

		NON PATENT LITERATURE DOCUMENTS (CONT.)	
Examiner Initials*	Cite No. 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	1.5
	A-27	CHOI, YANG-KYU et al.; "Sub-20nm CMOS FinFET Technologies"; 2001 IEEE, 4 pp	
	A-28	KEDZIERSKI, JAKUB et al.; "High-Performance Symmetric-Gate and CMOS-Compatible Vt Asymmetric-Gate FinFET Devi ces"; 2001; IEEE; 4 pp.	
	A-28	HISAMOTO, DIGH et al.; "FinFET – A Self-Aligned Double-Gate MOSFET Scalable to 20 nm"; IEEE Transactions on Electron Devices; Vol. 47, No. 12, December 2000, pp 2320-2325.	
	A-30	TANAKA, TETSU et al; "Ultrafast Operation of V _{th} -Adjusted P+n+ Double Gate SOI MOSFET's; IEEE Electron Device Letters, Vol 15, No. 10, October 1994; pgs 386-388.	
	A-31	CHAN et al.; "A True Single-Transistor Oxide-Nitride-Oxide EEPROM Device"; IEEE Electron Device Letters; March 1987; pp 93-95; Vol. EDL-8, No. 3.	
	A-32	GONZALEZ, FERNANDO Sr. et al.; "A Dynamic Source-Drain Extension (DSDE) MOSFET Using a Separately Biased Conductive Spacer"; pp 645-648	
	A-33	KIM, KEUNWOO et al.; "Double-Gate CMOS Symmetrical – Versus Asymmetrical-Gate Devices"; IEEE Transactions On Electron Devices, Vol 48, No. 2; February 2001; pp 294-299.	
	A-34	FOSSUM, JERRY G. et al.; "Extraordinarily High Drive currents in Asymmetrical Double-Gate MOSFETS"; Superlattices and Microstructures, Vol 28, No. 5/6, 2000, 2000 Academic Press, pp 525-530.	

Examiner	Date	
Signature	Considered	

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